What is claimed is:

1. A method for low-density parity-check (LDPC) encoding of data, the method comprising:
defining a first MxN parity check matrix;
generating, based on the first parity check matrix, a second parity check matrix having an MxM triangular sub-matrix; and,
mapping the data into an LDPC code word based on the second parity check matrix.

2. A method as claimed in claim 1, further comprising eliminating 4-cycles from the second matrix.

3. A method as claimed in claim 1, wherein the defining of the parity check matrix comprises cyclically shifting of rows of the first matrix.

4. A method as claimed in claim 1, comprising setting entries along the main diagonal of the MXM triangular sub-matrix to the same value.

5. Apparatus for low-density parity-check (LDPC) encoding of data, the apparatus comprising:
matrix definition logic for defining a first MxN parity check; a triangular matrix generator for generating a second parity check matrix based on the first parity check matrix; the second parity check matrix having an MxM triangular sub-matrix; and, an encoder for mapping the data into an LDPC code word based on the second parity check matrix.

6. Apparatus as claimed in claim 5, wherein the triangular matrix generator, in use, eliminates 4-cycles from the second matrix.

7. Apparatus as claimed in claim 5, wherein the matrix definition logic, in use, cyclically shifts rows of the first matrix.

8. Apparatus as claimed in claim 5, wherein the matrix definition logic, in use sets entries along the main diagonal of the MXM sub-matrix to the same value.

9. A computer program product for low-density parity-check (LDPC) encoding of data, the computer program product comprising a machine readable storage medium storing computer program code which, when loaded in a programmable data processor, configures the processor to perform the steps of:

defining a first MxN parity check matrix;

generating, based on the first parity check matrix, a second parity check matrix having an MxM triangular sub-matrix; and,

mapping the data into an LDPC code word based on the second parity check matrix.

10. A computer program product as claimed in claim 9, further comprising eliminating 4-cycles from the second matrix.

11. A computer program product as claimed in claim 9, wherein the defining of the parity check matrix comprises cyclically shifting of rows of the first matrix.

12. A computer program product as claimed in claim 9, comprising setting entries along the main diagonal of the MXM triangular sub-matrix to the same value.

13. A data transmitter for transmitting data received from an information source via a communications channel, the data being encoded by the transmitter into a low-density parity-check (LDPC) code word, the transmitter comprising: matrix definition logic for defining a first MxN parity check matrix; a triangular matrix generator for generating a second parity check matrix based on the first parity check matrix; the second parity check matrix having an MxM triangular sub-matrix; and, an encoder for mapping the data into an LDPC code word based on the second parity check matrix.

14. A data storage system for storing data received from an information source in a data storage channel, the data being encoded by the system into a low-density parity-check (LDPC) code word, the system comprising: matrix definition logic for defining a first MxN parity check matrix; a triangular matrix generator for generating a second parity check matrix based on the first parity check matrix; the second parity check matrix having an MxM triangular sub-matrix; and, an encoder for mapping the data into an LDPC code word based on the second parity check matrix.